Remarks

Thorough examination by the Examiner is noted and appreciated. Examiner has indicated Claims 1-31 are pending in the Application and that Claims 21-31 have been withdrawn from consideration. Applicants respectfully assume that Examiner meant to say that claims 1-32 are pending and that claims 21-32 have been withdrawn and have proceeded on that assumption. Claims 1-10 have been rejected. Applicants gratefully acknowledge Examiners allowance of claims 11-20.

The Specification has been amended to correct grammatical errors.

Claims 3 and 11 have been amended to correct grammatical and typographical errors.

New claims have been amended to clarify Applicants invention to achieve indicated allowable subject matter.

Support for the amended and newly added claims are found in the original claims and/or the Specification. No new matter has been added.

Claim Rejections under 35 USC 103

Claims 1-10 stand rejected under 35 USC 103(a) as being unpatentable over Iwamatsu (US 6,215,197) in view of Applicants alleged admitted prior art.

Iwamatsu discloses a process for forming isolation trenches in an active area (memory cell area) (see item 11B, Figure 1) adjacent an inactive area having an alignment mark area) (see item 11A) and a peripheral circuit area (i.e., also an active area).

The method of Iwamatsu is intended to **create a sufficient height difference** in a pre-etching step (also referred to as a reverse mask etch) prior to a CMP process **in order to improve the detection of the alignment mark** for more accurate alignment of gate electrode patterns formed over the active area (see Abstract; col 2, lines 18-29).

Examiner refers to the embodiment shown in Figures 12-17, e.g., item 52 of Figure of Figure 14 to assert that Iwamatsu teaches "forming a resist layer comprising patterned portions disposed between the active area trenches and the at least one

inactive area trench;" and refers to Figures 12-15, col 13, lines 61=col 14, line 40 to make the assertion that Iwamatsu teaches "planarizing the wafer process surface wherein the active area trenches and the at least one inactive area trench are substantially co-planar."

Applicants respectfully assert that nowhere does Iwamatsu teach "forming a resist layer comprising patterned portions disposed between the active area trenches and the at least one inactive area trench". Iwamatsu teaches that resist 52 is formed on "**convex portions**" "in the vicinity region of the peripheral portions of trenches 10A (10A1 and 10A2)" and does not show, teach or suggest any patterned portions between the active and inactive areas.

Moreover, Applicants respectfully assert that nowhere does Iwamatsu disclose or teach "planarizing the wafer process surface wherein the active area trenches and the at least one inactive area trench are substantially co-planar." Rather, such a step would **defeat the purpose** of Iwamatsu which is to **create a height difference** between the alignment mark area (inactive area) and the active area (memory cell area).

On the other hand, the fact that Applicants disclose that it is conventional to form a laser marked identification area at the periphery of a wafer and further disclose that a **problem presented thereby is a step height** that is created in prior art processes between the laser marked identification area and adjacent active areas cannot further help Examiner in making out a *prima facie* case of obviousness.

Even assuming *arguendo* a proper motivation for combining teachings of Iwamatsu with the prior art and problem discussed by Applicants; such combination does not produce Applicants disclosed and claimed invention of "wherein the active area trenches and the at least one inactive area trench are **substantially co-planar**". Moreover, such combination **presents the very problem** that Applicants solve and would make the method of Iwamatsu, who teaches **creating a step height** (non-coplanar) between the active areas and non-active area (alignment mark area) unsuitable for its intended purpose.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior

art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

Conclusion

Applicants gratefully acknowledge Examiners indication of allowable subject matter in claims 11-20 and have corrected a grammatical error in claim 11. Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in condition for allowance for any reason, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

TUNG & ASSOCIATES

Randy W. Tung
Reg. No. 31,311
Telephone: (248) 540-4040